**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IV. Remarks

Rejection of Claims 1-14 Under 35 U.S.C. §112, First Paragraph.

Applicant has amended claims 1, 7, and 14 to change "data generating circuit" to "data storing circuit". These amendments are believed to address any issues regarding lack of support for the term "data circuit in the core region" as the specification refers to "a data storing circuit ... formed within the core region".[1]

Rejection of Claim 1-14 Under 35 U.S.C. §112, Second Paragraph.

Applicant has amended claims 1, 2, 7, and 11 to address this ground for rejection. Applicant believes that the amendments clarify the claims and make them definite.

Rejection of Claims 15-21 Under 35 U.S.C. §102 based on Applicant's Background Art (*BACKGROUND ART*).

The invention of claim 15 is directed to a memory controller connected to a semiconductor memory device that includes a predetermined number "m" data input terminals, a predetermined number "n" signal input terminals (where m > n), a data storing circuit for receiving digital data from the data input terminals. Also included are n input delay circuits that delay received device input clock signals from the semiconductor memory device, m input holding circuits that hold the input data in synchronism with the input strobe signals generated by the input delay circuits, and m data input wirings. Each data input wiring transmits an input data value from one data input terminal to a corresponding input holding circuit. The memory controller further includes m signal input wirings transmitting one input strobe signal from one input delay circuit to a corresponding input holding circuit. The data input wiring and signal input wiring for the same corresponding input holding circuit are equal in length.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

[1] See page 13, lines 12-15 of the Specification

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Claim 15 recites the data input wiring and signal input wiring for the same corresponding input holding circuit are equal in length.

The rejection reasoning argues that wirings 225 of the *BACKGROUND ART* "have the same length". This is correct. However, wirings 225 can be wirings 225 describe output data signals. Wirings 225 are not a signal input wiring. A signal input wiring would be wiring 222, for example. Thus, the *BACKGROUND ART* does not show the data input wiring and signal input wiring for the same corresponding input holding circuit are equal in length.

Because the *BACKGROUND ART* does not show all elements of claim 1, this ground of rejection is traversed.

Claims 1, 2, 7, 11, 17, and 21 have been amended, not in response to the prior art but to address informalities and clarify the invention. The present claims 1-21 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

March 12, 2007

Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314